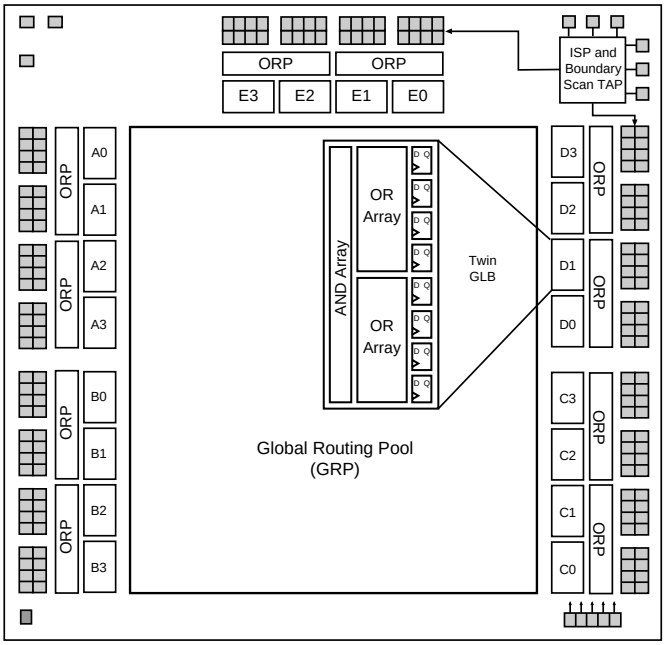
ispLSI® 3160

In-System Programmable High Density PLD

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 160 I/O Pins**
  - **— 7000 PLD Gates**
  - **— 320 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— fmax = 125 MHz Maximum Operating Frequency**
  - **— tpd = 7.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— 5V In-System Programmability (ISP™) Using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 3160 is a High-Density Programmable Logic Devices containing 320 Registers, 160 Universal I/O pins, five Dedicated Clock Input Pins, five Output Routing Pools (ORP) and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3160 features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 3160 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 3160 device is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...E3. There are a total of 20 of these Twin GLBs in the ispLSI 3160 device. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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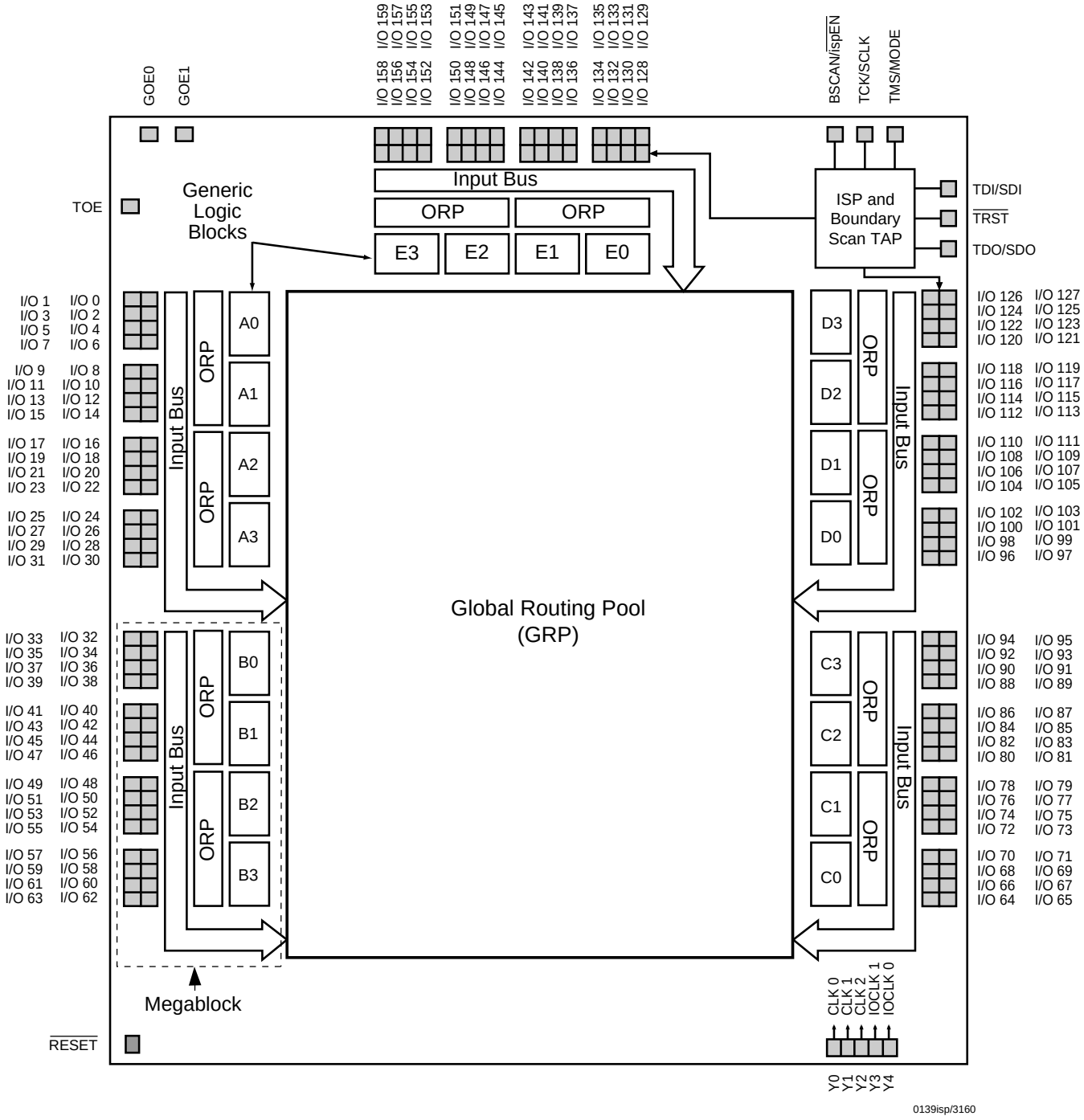
Functional Block Diagram

Figure 1. ispLSI 3160 Functional Block Diagram



Description (Continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 160 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 160 I/O cells are grouped into ten sets of 16 bits. Pairs of these I/O groups are associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. The PTOE can be generated by any GLB in the Megablock. Each I/O cell can select one of the seven available OEs (two Global OEs and five PTOEs).

Four Twin GLBs, 32 I/O cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of one pair of Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI 3160 device contains five of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 3160 device are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI 3160 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI 3160 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI 3160

Attribute	Quantity
Twin GLBs	20
Registers	320
I/O Pins	160
Global Clocks	5
Global OE	2
Test OE	1

Table 1-0003A/3160

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/3160

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/3160

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3160

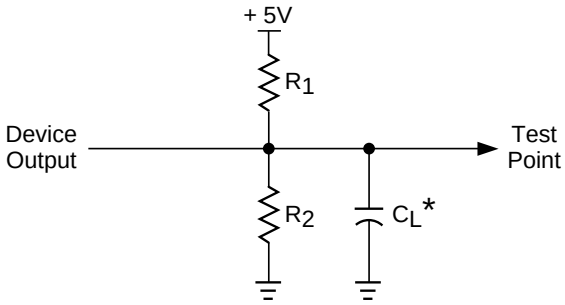
Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See Figure 2	

Table 2-0003/3160

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A/3160

Output Load conditions (See Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	Bscan/$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	–	275	–	mA

Table 2-0007/3160

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using ten 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARA-METER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-125		-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	7.5	—	10.0	—	15.0	ns
tpd2	A	2	Data Propagation Delay	—	10.0	—	13.0	—	18.0	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	125	—	100	—	70.0	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	95.0	—	87.0	—	50.0	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	125	—	100	—	83.0	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.0	—	5.5	—	9.0	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	4.5	—	5.0	—	9.0	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0.0	—	0.0	—	0.0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	6.0	—	6.5	—	11.0	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	5.0	—	5.5	—	10.0	ns
th2	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	0.0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	10.0	—	13.5	—	15.0	ns
trw1	—	13	Ext. Reset Pulse Duration	5.5	—	6.5	—	12.0	—	ns
tptoeen	B	14	Input to Output Enable	—	12.0	—	15.0	—	18.0	ns
tptoedis	C	15	Input to Output Disable	—	12.0	—	15.0	—	18.0	ns
tgoeen	B	16	Global OE Output Enable	—	7.0	—	9.0	—	12.0	ns
tgoedis	C	17	Global OE Output Disable	—	7.0	—	9.0	—	12.0	ns
ttoeen	—	18	Test OE Output Enable	—	8.0	—	12.0	—	15.0	ns
ttoedis	—	19	Test OE Output Disable	—	8.0	—	12.0	—	15.0	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	4.0	—	5.0	—	6.0	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	4.0	—	5.0	—	6.0	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	4.0	—	4.5	—	5.0	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0.0	—	0.0	—	0.0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.3160.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
tiobp	24	I/O Register Bypass	—	0.8	—	1.3	—	4.0	ns
tiolat	25	I/O Latch Delay	—	7.4	—	9.2	—	13.5	ns
tiosu	26	I/O Register Setup Time before Clock	4.3	—	4.8	—	5.8	—	ns
tioh	27	I/O Register Hold Time after Clock	-1.6	—	-1.6	—	-2.5	—	ns
tioco	28	I/O Register Clock to Out Delay	—	3.1	—	4.7	—	8.5	ns
tior	29	I/O Register Reset to Out Delay	—	5.5	—	5.8	—	8.0	ns
GRP									
tgrp	30	GRP Delay	—	1.8	—	2.3	—	2.6	ns
GLB									
t4ptbp	31	4 Product Term Bypass Path Delay (Comb.)	—	3.1	—	3.1	—	4.2	ns
t4ptbr	32	4 Product Term Bypass Path Delay (Reg.)	—	3.2	—	3.2	—	3.4	ns
t1ptxor	33	1 Product Term/XOR Path Delay	—	3.9	—	4.1	—	4.6	ns
t20ptxor	34	20 Product Term/XOR Path Delay	—	4.0	—	4.0	—	4.5	ns
txoradj	35	XOR Adjacent Path Delay[3]	—	4.3	—	4.3	—	5.3	ns
tgbp	36	GLB Register Bypass Delay	—	0.6	—	1.6	—	1.7	ns
tgsu	37	GLB Register Setup Time before Clock	-0.2	—	-0.2	—	0.9	—	ns
tgh	38	GLB Register Hold Time after Clock	4.6	—	5.6	—	8.0	—	ns
tgco	39	GLB Register Clock to Output Delay	—	1.6	—	0.6	—	2.9	ns
tgro	40	GLB Register Reset to Output Delay	—	4.7	—	5.1	—	5.1	ns
tptre	41	GLB Product Term Reset to Register Delay	—	4.0	—	4.0	—	4.2	ns
tptoe	42	GLB Product Term Output Enable to I/O Cell Delay	—	5.5	—	5.5	—	5.3	ns
tptck	43	GLB Product Term Clock Delay	3.0	3.6	3.0	3.6	3.2	4.0	ns
ORP									
torp	44	ORP Delay	—	1.2	—	1.2	—	1.9	ns
torpbp	45	ORP Bypass Delay	—	0.2	—	0.7	—	0.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Timing Int.3160.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
tob	46	Output Buffer Delay	—	1.6	—	2.6	—	3.3	ns
tobs	47	Output Buffer Delay, Slew Limited Adder	—	11.6	—	12.6	—	13.3	ns
toen	48	I/O Cell OE to Output Enabled	—	3.9	—	5.9	—	6.1	ns
todis	49	I/O Cell OE to Output Disabled	—	3.9	—	5.9	—	6.1	ns
Clocks									
tgy0/1/2	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line	0.6	1.1	1.1	1.1	1.9	1.9	ns
tioy3/4	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	0.3	1.6	0.3	1.6	0.8	2.5	ns
Global Reset									
tgr	52	Global Reset to GLB and I/O Registers	—	3.5	—	4.6	—	4.7	ns
tgoe	53	Global OE Pad Buffer	—	3.1	—	3.1	—	5.9	ns
ttoe	54	Test OE Pad Buffer	—	4.1	—	6.1	—	8.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

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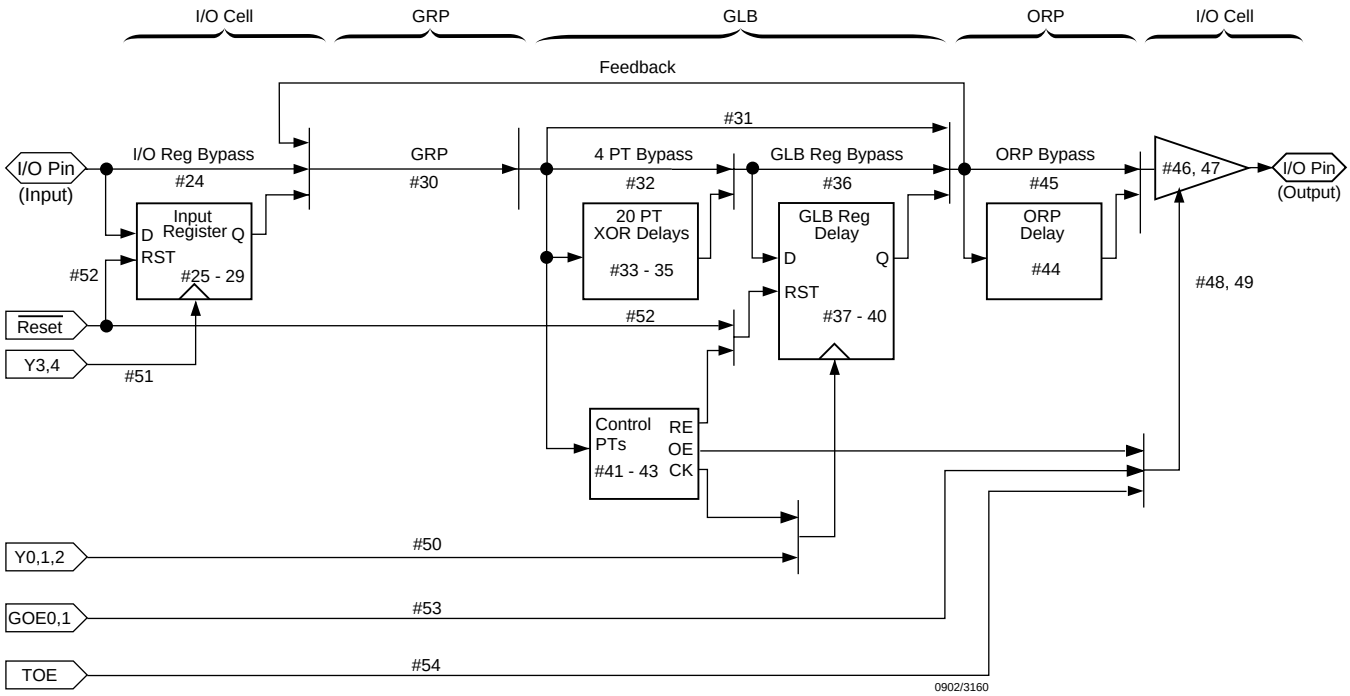
ispLSI 3160 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
0.8ns	=	(0.8 + 1.8 + 4.0) + (-0.2) - (0.8 + 1.8 + 3.0)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
4.2ns	=	(0.8 + 1.8 + 3.6) + (4.6) - (0.8 + 1.8 + 4.0)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #43) + (#39) + (#44 + #46)
10.1ns	=	(0.8 + 1.8 + 3.6) + (1.1) + (1.2 + 1.6)

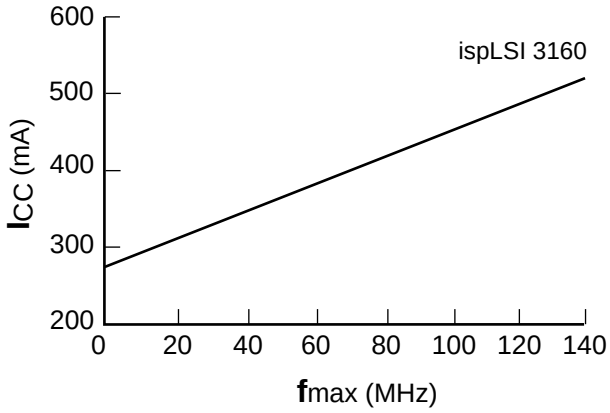
Table 2-0042/3160

Note: Calculations are based upon timing specifications for the ispLSI 3160-125L.

Power Consumption

Power consumption in the ispLSI 3160 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of ten 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 3160 using the following equation:

I_{CC} = 50 + (# of PTs * 0.73) + (# of nets * Max. freq * 0.0105) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/3160

Package Thermal Characteristics

For the ispLSI 3160-125LB272, it is strongly recommended that the actual Icc be verified to ensure that the maximum junction temperature (T_J) with power supplied is not exceeded. Depending on the specific logic design and clock speed, airflow may be required to satisfy the maximum allowable junction temperature (T_J) specification. Please refer to the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM for additional information on calculating T_J.

Signal Descriptions

Signal Name	Description
GOE0, GOE1	Global Output Enable input pins.
I/O	Input/Output Pins – These are the general purpose I/O pins used by the logic array.
TOE	Test Output Enable pin. This pin tristates all I/O pins when a logic low is driven.
$\overline{\text{RESET}}$	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3, Y4	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the I/O cells on the device.
BSCAN/$\overline{\text{ispEN}}$	Input – Dedicated in-system programming enable input pin. When this pin is high, the BSCAN TAP controller pins TMS, TDI, TDO and TCK are enabled. When this pin is brought low, the ISP State Machine control pins MODE, SDI, SDO and SCLK are enabled. High-to-low transition of this pin will put the device in the programming mode and put all I/O pins in the high-Z state.
TDI/SDI	Input – This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the ISP State Machine.
TCK/SCLK	Input – This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE	Input – This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP State Machine.
$\overline{\text{TRST}}$	Input – Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO	Output – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the ISP data. When $\overline{\text{ispEN}}$ is high, it functions as Test Data Out.
GND	Ground (GND)
VCC	Vcc
NC[1]	No Connect.

Signal Locations

Signal	208-Pin PQFP	272-Ball BGA
GOE0, GOE1	133, 134	J19, J18
TOE	30	M3
$\overline{\text{RESET}}$	28	M1
Y0, Y1, Y2, Y3, Y4	132, 130, 129, 128, 127	J20, K19, K20, L20, L18
BSCAN/$\overline{\text{ispEN}}$	27	L4
TDI/SDI	25	L3
TCK/SCLK	24	L2
TMS/MODE	23	L1
$\overline{\text{TRST}}$/NC[1]	29	M2
TDO/SDO	185	C10
GND	11, 26, 42, 53, 65, 78, 92, 104, 115, 131, 146, 157, 169, 183, 196, 208	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17
VCC	14, 39, 58, 80, 99, 118, 143, 162, 181, 203	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15
NC[1]	76, 77, 79, 81, 180, 182, 184	A2, A6, A10, A14, A19, A20, B1, B2, B4, B10, B14, B16, B17, B18, B19, C2, C3, C5, C7, C16, D2, D3, F18, F19, G3, H3, K1, K17, K18, P20, R2, R3, R20, U11, U19, V5, V7, V11, V14, V18, V19, W2, W3, W7, W11, W15, W17, W19, W20, Y1, Y2, Y4, Y10, Y11, Y18, Y20

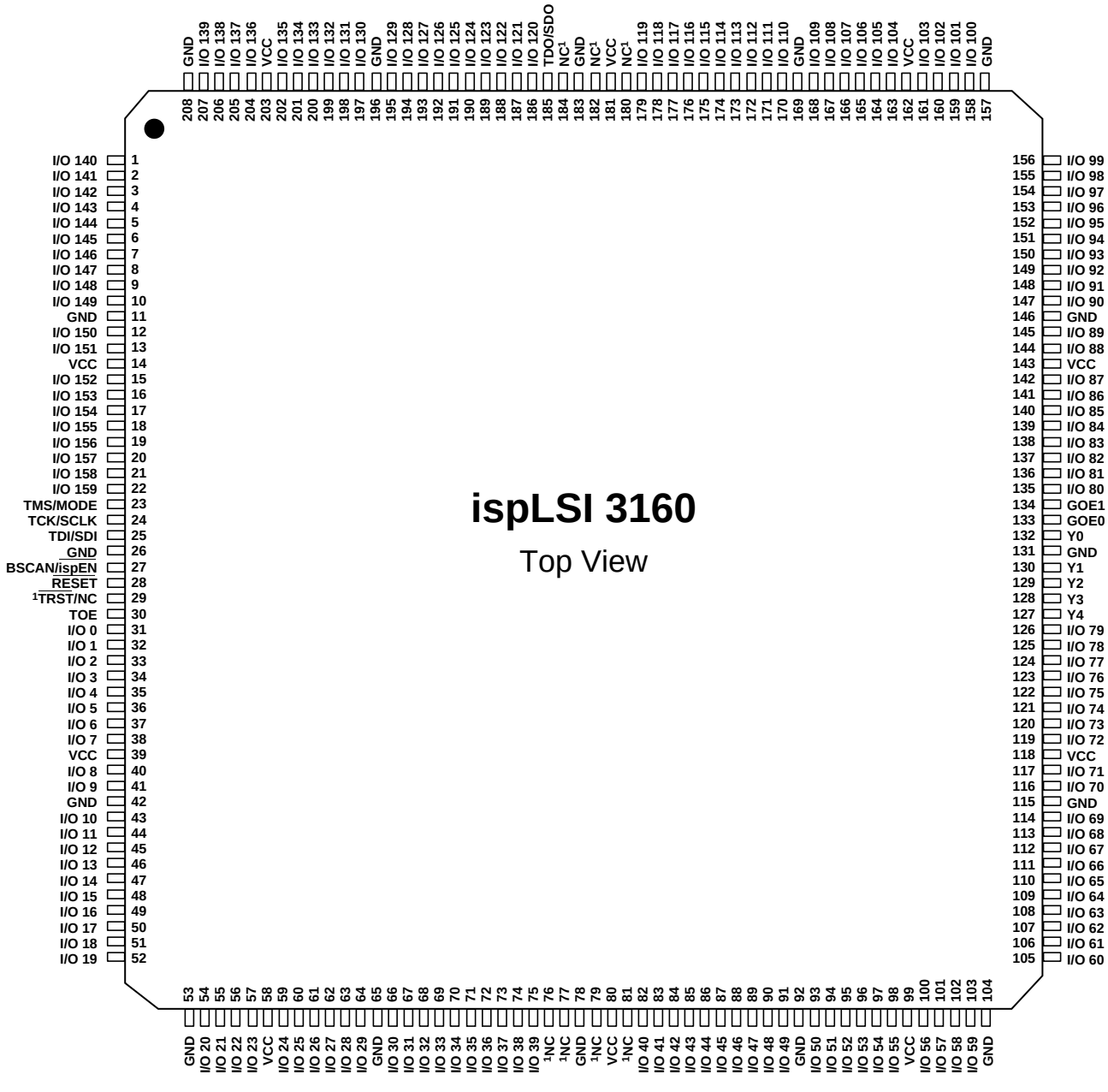
1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations

Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA
I/O 0	31	M4	I/O 32	68	W8	I/O 64	109	T18	I/O 96	153	D18	I/O 128	194	A7
I/O 1	32	N1	I/O 33	69	Y8	I/O 65	110	T19	I/O 97	154	C19	I/O 129	195	B7
I/O 2	33	N2	I/O 34	70	U9	I/O 66	111	T20	I/O 98	155	B20	I/O 130	197	B6
I/O 3	34	N3	I/O 35	71	V9	I/O 67	112	R18	I/O 99	156	C18	I/O 131	198	A5
I/O 4	35	P1	I/O 36	72	W9	I/O 68	113	P17	I/O 100	158	C17	I/O 132	199	D7
I/O 5	36	P2	I/O 37	73	Y9	I/O 69	114	R19	I/O 101	159	D16	I/O 133	200	C6
I/O 6	37	R1	I/O 38	74	W10	I/O 70	116	P18	I/O 102	160	A18	I/O 134	201	B5
I/O 7	38	P3	I/O 39	75	V10	I/O 71	117	P19	I/O 103	161	A17	I/O 135	202	A4
I/O 8	40	T1	I/O 40	82	Y12	I/O 72	119	N18	I/O 104	163	A16	I/O 136	204	A3
I/O 9	41	P4	I/O 41	83	W12	I/O 73	120	N19	I/O 105	164	C15	I/O 137	205	D5
I/O 10	43	T2	I/O 42	84	V12	I/O 74	121	N20	I/O 106	165	D14	I/O 138	206	C4
I/O 11	44	U1	I/O 43	85	U12	I/O 75	122	M17	I/O 107	166	B15	I/O 139	207	B3
I/O 12	45	T3	I/O 44	86	Y13	I/O 76	123	M18	I/O 108	167	A15	I/O 140	1	E4
I/O 13	46	U2	I/O 45	87	W13	I/O 77	124	M19	I/O 109	168	C14	I/O 141	2	C1
I/O 14	47	V1	I/O 46	88	V13	I/O 78	125	M20	I/O 110	170	C13	I/O 142	3	D1
I/O 15	48	T4	I/O 47	89	Y14	I/O 79	126	L19	I/O 111	171	B13	I/O 143	4	E3
I/O 16	49	U3	I/O 48	90	W14	I/O 80	135	J17	I/O 112	172	A13	I/O 144	5	E2
I/O 17	50	V2	I/O 49	91	Y15	I/O 81	136	H20	I/O 113	173	D12	I/O 145	6	E1
I/O 18	51	W1	I/O 50	93	Y16	I/O 82	137	H19	I/O 114	174	C12	I/O 146	7	F3
I/O 19	52	V3	I/O 51	94	U14	I/O 83	138	H18	I/O 115	175	B12	I/O 147	8	G4
I/O 20	54	W4	I/O 52	95	V15	I/O 84	139	G20	I/O 116	176	A12	I/O 148	9	F2
I/O 21	55	V4	I/O 53	96	W16	I/O 85	140	G19	I/O 117	177	B11	I/O 149	10	F1
I/O 22	56	U5	I/O 54	97	Y17	I/O 86	141	F20	I/O 118	178	C11	I/O 150	12	G2
I/O 23	57	Y3	I/O 55	98	V16	I/O 87	142	G18	I/O 119	179	A11	I/O 151	13	G1
I/O 24	59	W5	I/O 56	100	U16	I/O 88	144	E20	I/O 120	186	D10	I/O 152	15	H2
I/O 25	60	Y5	I/O 57	101	V17	I/O 89	145	G17	I/O 121	187	A9	I/O 153	16	H1
I/O 26	61	V6	I/O 58	102	W18	I/O 90	147	E19	I/O 122	188	B9	I/O 154	17	J4
I/O 27	62	U7	I/O 59	103	Y19	I/O 91	148	D20	I/O 123	189	C9	I/O 155	18	J3
I/O 28	63	W6	I/O 60	105	U18	I/O 92	149	E18	I/O 124	190	D9	I/O 156	19	J2
I/O 29	64	Y6	I/O 61	106	T17	I/O 93	150	D19	I/O 125	191	A8	I/O 157	20	J1
I/O 30	66	Y7	I/O 62	107	V20	I/O 94	151	C20	I/O 126	192	B8	I/O 158	21	K2
I/O 31	67	V8	I/O 63	108	U20	I/O 95	152	E17	I/O 127	193	C8	I/O 159	22	K3

Pin Configuration

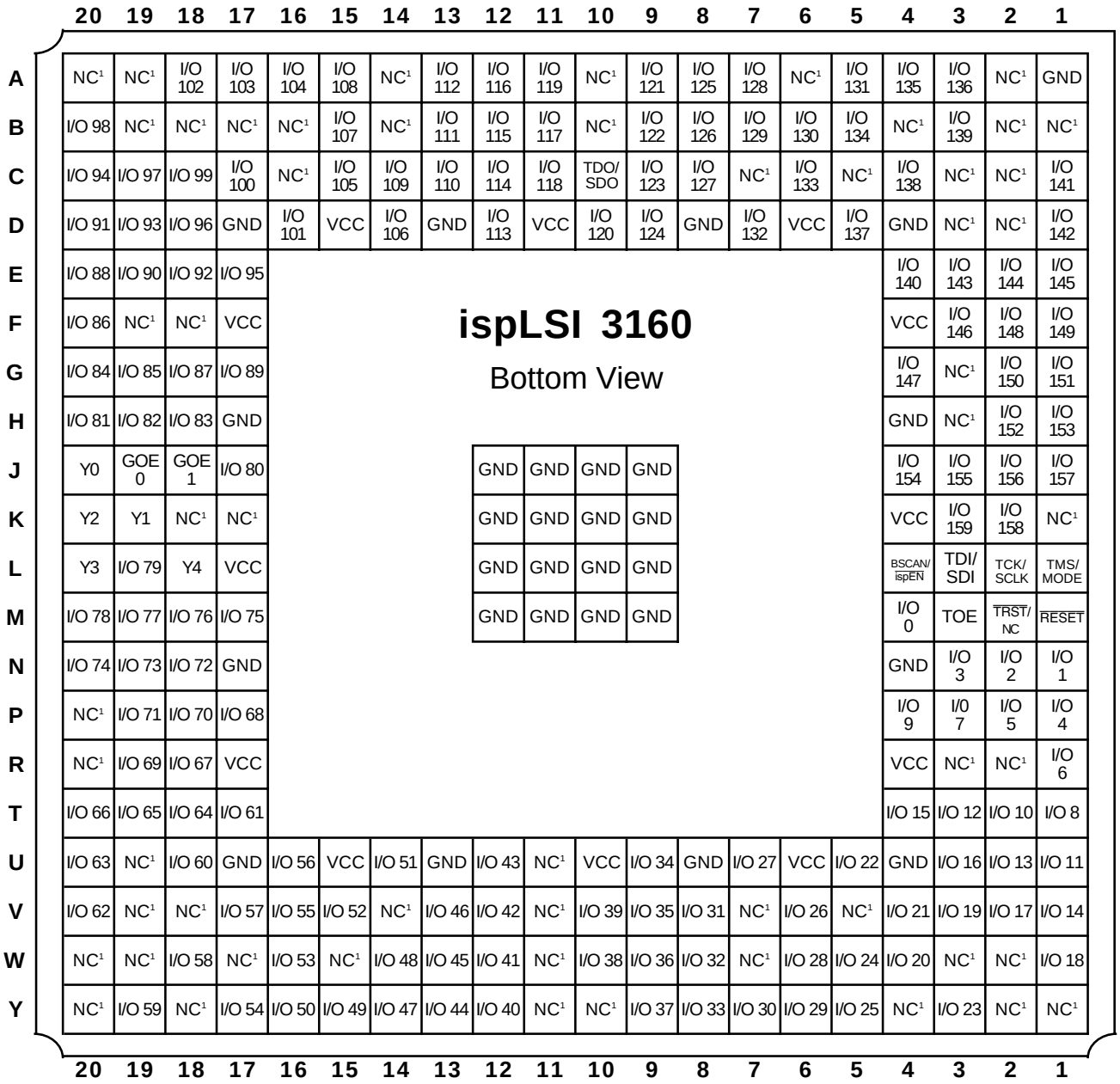
ispLSI 3160 208-Pin PQFP (with Heat Spreader) Pinout Diagram



1. NC pins are not to be connected to any active signal, VCC or GND.

Signal Configuration

ispLSI 3160 272-Ball BGA Signal Diagram



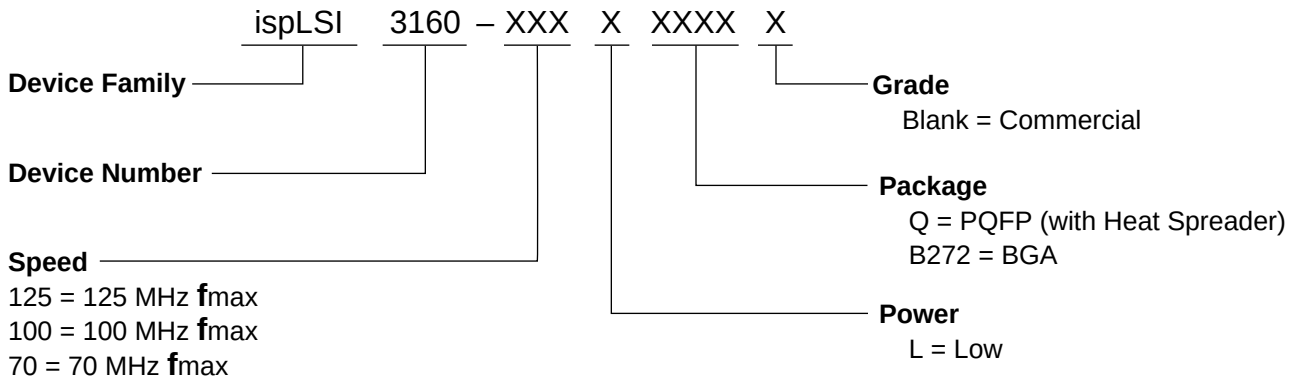
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	NC[1]	NC[1]	I/O 102	I/O 103	I/O 104	I/O 108	NC[1]	I/O 112	I/O 116	I/O 119	NC[1]	I/O 121	I/O 125	I/O 128	NC[1]	I/O 131	I/O 135	I/O 136	NC[1]	GND	A
B	I/O 98	NC[1]	NC[1]	NC[1]	NC[1]	I/O 107	NC[1]	I/O 111	I/O 115	I/O 117	NC[1]	I/O 122	I/O 126	I/O 129	I/O 130	I/O 134	NC[1]	I/O 139	NC[1]	NC[1]	B
C	I/O 94	I/O 97	I/O 99	I/O 100	NC[1]	I/O 105	I/O 109	I/O 110	I/O 114	I/O 118	TDO/ SDO	I/O 123	I/O 127	NC[1]	I/O 133	NC[1]	I/O 138	NC[1]	NC[1]	I/O 141	C
D	I/O 91	I/O 93	I/O 96	GND	I/O 101	VCC	I/O 106	GND	I/O 113	VCC	I/O 120	I/O 124	GND	I/O 132	VCC	I/O 137	GND	NC[1]	NC[1]	I/O 142	D
E	I/O 88	I/O 90	I/O 92	I/O 95													I/O 140	I/O 143	I/O 144	I/O 145	E
F	I/O 86	NC[1]	NC[1]	VCC													VCC	I/O 146	I/O 148	I/O 149	F
G	I/O 84	I/O 85	I/O 87	I/O 89													I/O 147	NC[1]	I/O 150	I/O 151	G
H	I/O 81	I/O 82	I/O 83	GND													GND	NC[1]	I/O 152	I/O 153	H
J	Y0	GOE 0	GOE 1	I/O 80													I/O 154	I/O 155	I/O 156	I/O 157	J
K	Y2	Y1	NC[1]	NC[1]													VCC	I/O 159	I/O 158	NC[1]	K
L	Y3	I/O 79	Y4	VCC													BSCAN/ ispEN	TDI/ SDI	TCK/ SCLK	TMS/ MODE	L
M	I/O 78	I/O 77	I/O 76	I/O 75													I/O 0	TOE	TRST/ NC	RESET	M
N	I/O 74	I/O 73	I/O 72	GND													GND	I/O 3	I/O 2	I/O 1	N
P	NC[1]	I/O 71	I/O 70	I/O 68													I/O 9	I/0 7	I/O 5	I/O 4	P
R	NC[1]	I/O 69	I/O 67	VCC													VCC	NC[1]	NC[1]	I/O 6	R
T	I/O 66	I/O 65	I/O 64	I/O 61													I/O 15	I/O 12	I/O 10	I/O 8	T
U	I/O 63	NC[1]	I/O 60	GND	I/O 56	VCC	I/O 51	GND	I/O 43	NC[1]	VCC	I/O 34	GND	I/O 27	VCC	I/O 22	GND	I/O 16	I/O 13	I/O 11	U
V	I/O 62	NC[1]	NC[1]	I/O 57	I/O 55	I/O 52	NC[1]	I/O 46	I/O 42	NC[1]	I/O 39	I/O 35	I/O 31	NC[1]	I/O 26	NC[1]	I/O 21	I/O 19	I/O 17	I/O 14	V
W	NC[1]	NC[1]	I/O 58	NC[1]	I/O 53	NC[1]	I/O 48	I/O 45	I/O 41	NC[1]	I/O 38	I/O 36	I/O 32	NC[1]	I/O 28	I/O 24	I/O 20	NC[1]	NC[1]	I/O 18	W
Y	NC[1]	I/O 59	NC[1]	I/O 54	I/O 50	I/O 49	I/O 47	I/O 44	I/O 40	NC[1]	NC[1]	I/O 37	I/O 33	I/O 30	I/O 29	I/O 25	NC[1]	I/O 23	NC[1]	NC[1]	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212B/3160

Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 3160-125LQ	208-Pin PQFP
	125	7.5	ispLSI 3160-125LB272	272-Ball BGA
	100	10	ispLSI 3160-100LQ	208-Pin PQFP
	100	10	ispLSI 3160-100LB272	272-Ball BGA
	70	15	ispLSI 3160-70LQ	208-Pin PQFP
	70	15	ispLSI 3160-70LB272	272-Ball BGA

Table 2-0041B/3160